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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/553,841	04/21/2000	Khoi Phan	E0806	6614

7590 04/08/2005

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EXAMINER	
REKSTAD, ERICK J	
ART UNIT	**PAPER NUMBER**
2613	

DATE MAILED: 04/08/2005

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/553,841
Filing Date: April 21, 2000
Appellant(s): PHAN ET AL.

Himanshu S. Amin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/19/2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-23 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,843,527 SANADA 12/1/1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-7,10-12, and 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,089,763 to Sanada in view of US Patent 6,313,903 to Ogata.

[claims 1 and 15]

As shown in Figure 10, Sanada describes a system that visually monitors a semiconductor processing. The system monitors the spin coating process in the production of semiconductor wafers (Col 1 Lines 7-13). The system of Figure 10 includes an image collector (30) located at least partially within the chamber. The image collector collects energy reflected from inside the chamber and transmits a signal indicative of the interior of the chamber (Col 27 Lines 11-24).

Sanada is silent on the other processes required for the manufacturing of a semiconductor wafer, specifically the use of a developer chamber as required by the claims.

Ogata teaches a well known prior art fabrication process for a semiconductor device using semiconductor wafers as shown in Figure 13, wherein coating and

developing are essential steps in forming a semiconductor device (Col 1 Lines 5-37). As shown in Figure 13, Ogata teaches a coater and develop unit (13) is used to coat and develop a semiconductor wafer (Col 1 Line 11-Col 2 Line 21). Since Sanada is silent regarding the developing step, it speaks that this step is well known to those of ordinary skill. In fact, any well known technique could be used such as the combined coater/developer of Ogata. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the prior art fabrication process containing a combined coater/develop chamber as taught by Ogata in the system of Sanada in order to produce a complete semiconductor fabrication system with reduced cost, size and efficiently produce semiconductor devices by having less movement and alignment issues.

[claims 2, 3 and 17]

Sanada further teaches the system including a light source (40) that illuminates the interior of the develop chamber to enable the image collector to obtain a visible image of the interior of the chamber as required by claims 2 and 17(Col 27 Lines 25-37). Sanada further teaches the light source being a light emitting diode as required by claim 3 (Col 27 Line 33).

[claims 5 and 6]

Sanada further teaches the light source being selected so as not to expose the photoresist material (Col 27 Lines 32-37).

[claims 7 and 16]

Sanada teaches the image collector includes a camera module that collects the images and provides an electrical signal indicative of a visual representation of the interior of the chamber (Col 27 Lines 49-67).

[claims 10-12, 18]

Sanada teaches the camera and light source are connected to a viewing station (Confirmation Unit (50)) as required by claim 10. The viewing station provides a display of a visual representation of the interior of the chamber through a monitor (59) and provides controls for selectively controlling activation of the camera module and light source as required by claims 11, 12 and 18 (Figs 10 and 12, Col 27 Line 40-Col 28 Line 3).

[claim 19]

As shown in Figure 16, Sanada further teaches the method for visually monitoring an interior of a chamber. The method includes collecting visual images (T1), providing an image signal indicative thereof (T2) and displaying a visual representation of the interior (T3) (Col 31 Lines 4-45).

[claims 20 and 21]

Sanada further teaches including a light source (40) that illuminates the interior of the develop chamber to enable the image collector to obtain a visible image of the interior of the chamber as required by claim 20 (Col 27 Lines 25-37). Sanada further teaches the light source being a light emitting diode as required by claim 21 (Col 27 Line 33).

[claims 22 and 23]

Sanada teaches the camera and light source are connected to a viewing station (Confirmation Unit (50)) as required by claim 10. The viewing station provides a display of a visual representation of the interior of the chamber through a monitor (59) and provides controls for selectively controlling activation of the camera module and light source as required by claims 22 and 23 (Figs 10 and 12, Col 27 Line 40-Col 28 Line 3).

Claims 4, 8, 9, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanada and Ogata as applied to claims 1, 2, and 7 above, and further in view of US Patent 6,603,874 to Stern et al.

[claims 4,8,9,13, and 14]

Sanada and Ogata teach the system as described above for claims 1, 2 and 7. Sanada further teaches the use of an enclosed processing chamber and the use of LEDs for light (Col 27). Sanada and Ogata are silent on the benefits of fiber optics.

Stern teaches the benefit of using commercially available fiber optics to light an area of a semiconductor wafer and obtain images of a semiconductor wafer as required by claims 4 and 8 (Col 6, Lines 14-26). Stern further teaches the use of a faceted lens as required by claims 9 and 14 (Col 6 Lines 9-13). Stern also teaches that the input light for the fiber optic cable could be "white light" or a single color as generated by a LED or a single wavelength as generated by a laser (Col 5, Lines 5-10). Stern finally teaches that the fiber optic cable can be used with photodetectors in order to generate a video signal (Col 5 Lines 11-17, Fig 4A). It would have been obvious to one skilled in the art at the time of the invention to use fiber optic cable to transmit the light of an LED or laser in the system of Sanada and Ogata to take advantage of the commercially

available fiber optics as taught by Stern. It would have been obvious to one skilled in the art at the time of the invention to use photodetectors and fiber optic cable as a camera in the system of Sanada and Ogata in order to take advantage of the commercially available fiber optics as taught by Stern.

(11) Response to Argument

In regards to independent claim 1, Appellant argues that simply because the coater and developer of Ogata are one unit does not mean it would be obvious to combine the teachings of Sanada and Ogata to result in a develop chamber with an image collector that collects energy reflected therein and transmit a signal indicative of interior of the chamber as recited in the subject claims. Appellant further argues that since Sanada relates to visually monitoring a coating process and Ogata does not contemplate monitoring a develop process, there is no teaching, suggestion, motivation or desirability to combine these references to teach the subject claims.

The rejection of claim 1 under 35 U.S.C. 103(a) as shown above, teaches the desire to combine the coating process with the semiconductor wafer fabrication process of Ogata in order to provide a complete semiconductor wafer fabrication process using the coating process of Sanada. Further, claim 1 is silent on the requirement that the obtained energy by the image collector be related to the developing process. Therefore the combination of Sanada and Ogata in which the visual monitoring means only monitors the coating process in the coating and developing unit satisfies the requirements of claim 1.

In regards to claim 15, the Appellant argues the combination of Sanada and Ogata does not teach the imaging means for collecting images of an interior of an enclosed developer. Appellant further argues that since Sanada relates to visually monitoring a coating process and Ogata does not contemplate monitoring a develop process, there is no teaching, suggestion, motivation or desirability to combine these references to teach the subject claims.

The rejection of claim 15 under 35 U.S.C. 103(a) as shown above, teaches the desire to combine the coating process with the semiconductor wafer fabrication process of Ogata in order to provide a complete semiconductor wafer fabrication process using the coating process of Sanada. Further, claim 15 is silent on the requirement that the obtained energy by the image collector be related to the developing process. Therefore the combination of Sanada and Ogata in which the visual monitoring means only monitors the coating process in the coating and developing unit satisfies the requirements of claim 15.

In regards to claim 19, the Appellant argues the combination of Sanada and Ogata does not teach the imaging means for collecting images of an interior of a developer chamber. Appellant further argues that since Sanada relates to visually monitoring a coating process and Ogata does not contemplate monitoring a develop process, there is no teaching, suggestion, motivation or desirability to combine these references to teach the subject claims.

The rejection of claim 19 under 35 U.S.C. 103(a) as shown above, teaches the desire to combine the coating process with the semiconductor wafer fabrication process

of Ogata in order to provide a complete semiconductor wafer fabrication process using the coating process of Sanada. Further, claim 19 is silent on the requirement that the obtained energy by the image collector be related to the developing process. Therefore the combination of Sanada and Ogata in which the visual monitoring means only monitors the coating process in the coating and developing unit satisfies the requirements of claim 15.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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March 30, 2005

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